REMARKS

Claims 1-15 are pending in the application. In the Final Office Action mailed April 4, 2003, the Examiner indicated claims 8 and 15 comprised allowable subject matter. The Applicant thanks the Examiner for this indication of allowability. The remaining claims were rejected under 35 U.S.C. §102(e) as being anticipated by Pawlowski (U.S. Patent No. 5,787,475).

Applicant filed an Appeal in this case, asserting that Pawlowski does not anticipate the present invention because the device of Pawlowski, in response to a data output request, outputs an amount of data that corresponds to the amount of data that can be stored between neighboring output start addresses, and does not output an amount of data greater than the amount of data that can be stored between neighboring output start addresses.

This assertion was based on the premise that it was improper for the Examiner to read the "data storage device" of the present invention on the combination of Pawlowski's I/O module and main memory. The Board of Appeals, however, agreed with the Examiner's interpretation, and concluded that under such an interpretation, Pawlowski anticipates the present invention.

The Board of Appeals did state that if the Appellant's interpretation was correct, then Pawlowski does not anticipate the present invention. The present amendment, by the amendments to the independent claims, makes explicit that the claim scope covers a single integrated circuit unit (with the exception of claims 8, 15

indicated as allowable by the Examiner). Support for this amendment may be found on p. 3 of the originally filed application in the paragraph beginning at line 11.

Since the Board of Appeals indicated that a data storage device construed as a single device is not anticipated by Pawlowski, Applicants repeat the argumentation provided in the Appeal Brief for completeness in this response (amended as appropriate). Applicants further assert that the combination of the inventive elements related to a single integrated circuit unit are not obviated by Pawlowski for the reasons repeated below.

The last element of claim one requires that the data storage device *in a single integrated circuit unit* is configured such that:

> [the] selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request

Or, stated another way, when a data output request is provided to the device, it can output an amount of data larger than the amount of data between neighboring output start addresses that the device can be addressed by.

This is not the way that Pawlowski operates. In Pawlowski, the main memory 14 is segmented into a plurality of addressable cache lines 18 (4/55-56). If another system component (e.g., the I/O module 24) wants to read out data stored in the main memory 14, it has to address the main memory 14 using the start address of

one of the cache lines 18, and will receive the contents of a complete cache line (see, e.g., 6/15-19 and 50-59).

Therefore, the main memory 14 of Pawlowski is a (single IC unit) data storage device comprising the feature that the selectable output start addresses are spaced from one another such that the amount of data that can be stored between neighboring output start address corresponds to the amount of data output in response to a data output request.

Pawlowski does not permit the access of the single unit data storage device in amounts other than entire cache lines. According to Pawlowski, "All data transfers over the system bus must generally comprise an entire cache line worth of data." 4/59-60. Since the addressability of the cache memory 14 is only permitted at the beginning of the cache lines, it is only possible, according to Pawlowski, to get an amount of data *equal* to the spacing between neighboring start addresses per each request. In the relevant portions cited by the Examiner, e.g., 7/15-25, a "prefetch" of data beyond a single cache line may be performed, but this involves making a second or multiple requests of the memory: "... the data retriever may request a next consecutive cache line of data from main memory if the I/O controller has directed a second prefetch." 7/58-60.

The present invention primarily permits an overlap of the memory regions that can be retrieved based on the output start addresses of the memory device—i.e., multiple requests of the device may not be required when accessing an amount of

memory larger than the spacing of the possible output start addresses, which provides a fundamental advantage in terms of speed.

Similarly, independent claim 9 requires the outputting of stored data from the data storage device that is greater in quantity than the space between the neighboring output start addresses. Since Pawlowski only puts out a single cache line, and the neighboring output start addresses begin at the start of each cache line, Pawlowski does not anticipate independent claim 9 of the application.

Applicant previously asserted that the Examiner had improperly and equated the combination of Pawlowski's I/O module *and* main memory with the "data storage device" of claims 1 and 9 in the present invention. The Examiner indicated in his Response to Arguments section of the OA on p. 6 that a peripheral of Pawlowski can request (and receive) some arbitrary amount of data, e.g., greater than one addressable cache line, with a single request, thereby anticipating claims 1 & 9 of the present invention. Since the Board of Appeals supported the Examiner's interpretation, Applicants have now amended the independent claims to indicated that the device according to the invention constitutes a single IC unit (with the exception of claims 8 and 15).

Thus, under this claim construction, while it is true that a combination of Pawlowski's I/O module *and* main memory module can provide an arbitrary amount of data greater than one addressable cache line, this still requires two accesses to the main memory module itself, as discussed above, which is not a single IC unit.

The "device" of the present invention, as amended, would then only properly beequated with the main memory module of Pawlowski (as indicated by the Examiner on p. 3 under numbered paragraph 7, "Pawlowski discloses a data storage devices (main memory)..."); the I/O module of Pawlowski acts as a separate entity (as the Examiner calls out in line 3 of numbered paragraph 10 of the OA) that is between the memory and output terminals and is therefore not a part of the single IC unit. The disadvantage of Pawloski's use of the I/O module and main memory is that it involves an extra step—the main memory can only be accessed in cache line chunks and on cache line boundaries... it requires extra processing by the I/O module to discard extraneous data and concatenate data that spans cache line boundaries.

This is precisely the type of delay that the present invention seeks to address, i.e., requiring multiple accesses of the data storage device. Device claim 1 and method claim 9 both permit the access of more data in a single request than the distance between two start addresses. This is neither taught or suggested by Pawlowski, nor would the independent claims be obvious over Pawlowski.

For this reason, the Applicant asserts that the amended claim language clearly distinguishes over the prior art, and respectfully requests that the Examiner withdraw the §102(e) rejection from the present application. Applicant welcomes any suggestions by the Examiner with regard to claim language.

CONCLUSION

Inasmuch as each of the rejections have been overcome by the amendments and arguments presented, and all of the examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that this application be passed to issue.

Respectfully submitted,

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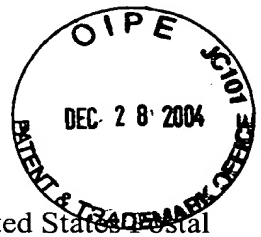

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Attorney Docket No.: **P00,0365-01**

Patent Application Entitled:

"DATA STORAGE DEVICE WITH OVERLAPPED BUFFERING SCHEME"

Signature of person Mailing application